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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/753,360	01/09/2004	Koji Yamaguchi	118290	6386
25944	7590	09/09/2004		
OLIFF & BERRIDGE, PLC P.O. BOX 19928 ALEXANDRIA, VA 22320			EXAMINER MALSAWMA, LALRINFAMKIM HMAR	
			ART UNIT 2825	PAPER NUMBER

DATE MAILED: 09/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/753,360	YAMAGUCHI, KOJI	
	Examiner	Art Unit	
	Lex Malsawma	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on Jan. 9, 2004 through May 28, 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-22 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-22 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 09 January 2004 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: reference label “34” specified in paragraphs 0128 and 0130 (in the substitute specification) are not shown in Fig. 7b. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled “Replacement Sheet” in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

2. Claims 5 and 11 are objected to because of the following informalities:

At claim 5, in line 7, “the conductive layers” should read “conductive layers”, otherwise there would be a lack of antecedent basis; and in line 11 (last line), “conductive layers” is interpreted as “the conductive layers” referring to the limitation in line 7.

At claim 11, in line 7, “the conductive layers” should read “conductive layers”, otherwise there would be a lack of antecedent basis; and in line 12, “conductive layers” is interpreted as “the conductive layers” referring to the limitation in line 7.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-4, 7, 10, 14 and 16-18 are rejected under 35 U.S.C. 102(e) as being anticipated by Poo et al. (US 2003/0230802 A1; hereinafter, “**Poo-I**”).

Regarding claim 1:

Poo-I discloses (in Figs. 6-8) a semiconductor device, comprising:

a semiconductor chip 10 having a main surface and a sidewall;

a wiring layer 28 formed on the main surface of the semiconductor chip; and

a conductive layer 31 for interlayer connections that is connected to the wiring layer 28

and formed in the side wall of the semiconductor chip (note Figs. 8-9 and paragraph 0048).

Therefore, this claim is anticipated.

Regarding claim 2:

Poo-I discloses (in Figs. 5-8) a semiconductor device, comprising:

a semiconductor chip 10 having a main surface;

electrode pads 20 formed on the main surface of the semiconductor chip;

grooves 40 formed in a section of the semiconductor chip that traverses in a thickness direction of the semiconductor chip;

conductive layers 31 filled in the grooves (note Fig. 5 and paragraph 0049); and
wiring layers 28 that connect the electrode pads 20 and the conductive layers 31.

Therefore, this claim is anticipated.

Regarding claim 3:

Poo-I discloses (in Figs. 6-9) a semiconductor device, comprising:

semiconductor chips 10A/10B stacked in layers (Fig. 9);

conductive layers 31 formed in side walls of the respective semiconductor chips to
provide interlayer connections among the semiconductor chips; and

wiring layers 28 formed on the main surfaces of the respective semiconductor chips and
connected to the conductive layers 31. Therefore, this claim is anticipated.

Regarding claim 4:

Poo-I discloses (in Figs. 5-9) a semiconductor device, comprising:

semiconductor chips 10A/10B stacked on layers (Fig. 9);

electrode pads 20 formed on main surfaces of the respective semiconductor chips;

grooves 40 formed in sections of the semiconductor chip that traverses in a thickness
direction of the semiconductor chips;

conductive layers 31 filled in the grooves (note Fig. 5 and paragraph 0049) to provide
interlayer connections among the semiconductor chips; and

wiring layers 28 that connect the electrode pads 20 and the conductive layers 31,
respectively. Therefore, this claim is anticipated.

Regarding claim 7:

Poo-I discloses (in Figs. 5-11) a semiconductor module, comprising:
an interposer substrate 88A (Fig. 11 and paragraph 0055) having a wiring layer 94 formed on a main surface thereof;
a semiconductor chip 10C connected to the wiring layer 94 and mounted on the interposer substrate;
grooves formed in a side wall of the interposer substrate 88A (Fig. 11) that traverses in a thickness direction of the interposer substrate; and
conductive layers 86 filled in the grooves. Therefore, this claim is anticipated.

Regarding claim 10:

Poo-I discloses (in Figs. 5-9) an electronic device, comprising:
semiconductor chips 10A/10B stacked on layers (Fig. 9);
electrode pads 20 formed on main surfaces of the respective semiconductor chips;
grooves 40 formed in sections of the semiconductor chip that traverses in a thickness direction of the semiconductor chips;
conductive layers 31 filled in the grooves (note Fig. 5 and paragraph 0049) to provide interlayer connections among the semiconductor chips;
wiring layers 28 that connect the electrode pads 20 and the conductive layers 31, respectively; and
an electronic component 42 (Fig. 7 and paragraph 0040, lines 5-&) connected to the semiconductor chips through the conductive layers. Therefore, this claim is anticipated.

Regarding claims 14 and 17:

Poo-I discloses (in Figs. 2, 3, 5-9) a method of manufacturing a semiconductor device/module, comprising:

- forming through holes 38 on cutting lines 14 of a semiconductor wafer;
- cutting the semiconductor wafer along the cutting lines into chips 10;
- stacking the semiconductor chips 10A/10B (Fig. 9) formed by the cutting; and
- filling conductive layers 31 in the through holes divided by the cutting. Therefore, these claims are anticipated.

Regarding claim 16:

Poo-I discloses (in Figs. 2, 3, 5-9) a method of manufacturing a semiconductor module, comprising:

- forming conductive layers 31 on sidewalls of a semiconductor chip 10; and
- providing interlayer connections 28 through the conductive layers formed on the side walls of the semiconductor chip. Therefore, this claim is anticipated.

Regarding claim 18:

Poo-I discloses (in Figs. 2, 3, 5-9) a method of manufacturing a semiconductor module, comprising:

- forming through electrodes 30A-C (Fig. 2 and paragraph 0045) on cutting lines 14 of a semiconductor wafer 8;
- cutting the semiconductor wafer along the cutting lines into chips 10; and

providing interlayer connections 28 among the semiconductor chips formed by the cutting via the through electrodes 31 (Figs. 7-8) that are cut by the cutting. Therefore, this claim is anticipated.

5. Claims 5, 11 and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Poo et al. (6,727,116 B2; hereinafter, "**Poo-II**").

Regarding claims 5 and 11:

Poo-II discloses a semiconductor module/chip, comprising:

semiconductor chips 10A-D(Fig. 17) stacked in layers;

electrode pads 20 (Fig. 3) formed on main surfaces of the respective chips;

grooves 40 (Fig. 3) formed in sections of the respective chips that traverse in a thickness direction of the semiconductor chips;

wiring layers 28 that connect the electrode pads and conductive layers 31 (Figs. 3-5);

pin-like terminals 88 (Figs. 17-19) embedded/inserted in the grooves and disposed in a stacking direction of the semiconductor chips;

an interposer substrate 82 with the pin-like terminals standing thereon (Figs 17-19 and Col. 12, lines 6-10);

the conductive layers 31 filled in the grooves with the pin-like terminals thereon (note Figs. 20-22); and

an electronic component 42 (Fig. 5 and Col. 7, lines 60-64) connected to the semiconductor chips through the conductive layers. Therefore, this claim is anticipated.

Regarding claim 20:

This claim is essentially drawn to a method for manufacturing the module in claim 5; accordingly, this claim is anticipated, since Poo-II discloses all recited process steps.

6. Claims 8, 9, 12, 13, 21 and 22 are rejected under 35 U.S.C. 102(b) as being anticipated by Shokrgozar et al. (5,434,745; hereinafter, "**Shokrgozar**").

Regarding claims 8 and 12:

Shokrgozar discloses a semiconductor module/device, comprising:
interposer substrates (17, 19, 26, 27) stacked in layers (Fig. 3 and Col. 5, lines 8-30);
wiring layers (2,6,10,12,16) formed on main surfaces of the interposer substrates (Fig. 1);
semiconductor chips 3 (Fig. 1) connected to the wiring layers and mounted on the interposer substrates;

grooves formed in side walls of the interposer substrates that transverse in a thickness direction of the interposer substrates (Figs. 1 and 3);

conductive layers 28 filled in the grooves to provide interlayer connections among the interposer substrates (Fig. 4 and Col. 5, lines 39-45);

recessed sections formed in back surfaces of the interposer substrates to store the semiconductor chips, i.e., one interposer substrate comprises base substrate 1 and frame 8, wherein recessed sections are formed by a combination of base substrate 1 and frame 8 (note Fig. 1); and

an electronic component inherently connected to the semiconductor chips through the conductive layers 28. Note that Shokrgozar discloses the module/device is generally directed to

memory chips such as SRAMs and DRAMs (note Col. 3, lines 15-24), wherein the conductive layers 28 are electrically connected attachment pads 29 of the flat pack assembly 30 (Fig. 4). The flat pack assembly must be connected to an electronic component, since the module/device on the flat pack is a memory chip. Therefore, these claims are anticipated.

Regarding claims 9 and 13:

Shokrgozar discloses a semiconductor module, comprising:

an intermediate substrate 8 (Fig. 1) having an opening section formed therein;
interposer substrates 1 stacked in layers through the intermediate substrate (Figs. 1-3);
wiring layers (2,6,10,12,16) formed on main surfaces of the interposer substrates (Fig. 1);
semiconductor chips 3 (Fig. 1) connected to the wiring layers and mounted on the interposer substrates;

first grooves 5 (Fig. 1) formed in side walls of the interposer substrates that transverse in a thickness direction of the interposer substrates;

second grooves 9 (Fig. 1) formed in a side wall of the intermediate substrate that traverses in a thickness direction of the intermediate substrate;

conductive layers 28 filled in the first and second grooves to provide interlayer connections among the interposer substrates through the intermediate substrate (Fig. 4 and Col. 5, lines 39-45); and

an electronic component inherently connected to the semiconductor chips through the conductive layers 28. Note that Shokrgozar discloses the module/device is generally directed to memory chips such as SRAMs and DRAMs (note Col. 3, lines 15-24), wherein the conductive layers 28 are electrically connected attachment pads 29 of the flat pack assembly 30 (Fig. 4). The

flat pack assembly must be connected to an electronic component, since the module/device on the flat pack is a memory chip. Therefore, these claims are anticipated.

Regarding claims 21 and 22:

These claims are essentially drawn to a method for manufacturing the module in claims 8 and 9; accordingly, these claims are anticipated, since Shokrgozar discloses all recited process steps.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over by **Poo-II** (6,727,116 B2) in view of **Shokrgozar** (5,434,745).

Regarding claim 6:

Poo-II anticipates the module of claim 5 but **lacks** the semiconductor chips being stacked through dielectric resin. Shokrgozar **teaches** a semiconductor module comprising a stack of chips, wherein all individual components of the module are stacked/attached through dielectric resin (note Col. 4, lines 36-46 and Col. 5, lines 3-6, 16-21, and 26-28). Note that the dielectric resin used by Shokrgozar allows a “stacked module” to be formed prior forming a conductive layer 28 within the grooves on the sidewalls of the “stacked module” (note Fig. 4 and Col. 5, lines 39-45). It would have been obvious to one of ordinary skill in the art to modify Poo-II by

Art Unit: 2825

utilizing dielectric resin as taught by Shokrgozar because the dielectric resin would allow a stack of chips to be attached in alignment prior to disposing/embedding the pin-like terminals in the sidewall grooves, i.e., initially acquiring an aligned stacked of chips would allowed the pin-like terminals to be embedded “evenly” into the grooves, such that contact is ensured between the pin-like terminals and each “metallized” groove on each chip.

9. Claims 15 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over by **Poo-II** (6,727,116 B2) in view of Brofman et al. (US 2002/0180013; hereinafter, “**Brofman**”).

Regarding claims 15 and 19:

Poo-II discloses a method of manufacturing a semiconductor device/module, comprising:
forming through holes 38 (Figs 10-14) within cutting lines of a semiconductor wafer;
cutting the semiconductor wafer along the cutting lines into chips 10A-D (Fig. 17-18 and Col. 10, lines 35-46);

stacking the semiconductor chips formed by the cutting; and
filling conductive layers 29 (Fig. 14 and Col. 10, lines 40-44) in the through holes that are divided by the cutting.

Poo-II **lacks** forming the through holes as recited in the current claims, i.e., Poo-II lacks forming trench sections on the cutting lines; forming dielectric films within the trench sections; forming an under barrier metal layer covering the dielectric films; and thinning a back surface of the wafer to make the trench sections penetrate to form the through holes. However, it is important to note that Poo-II specifically discloses (in Col. 9, lines 35-62) the through-holes may be formed by any known process, depending upon their heights, diameters and the pitch at which

the through-holes are spaced. Brofman **teaches** a method for efficiently forming vias through thin substrates, the method comprising: forming trench sections 117 (Fig. 3B) in a semiconductor wafer 110; forming dielectric films 120 (Fig. 3C) within the trench sections; forming an under barrier metal layer 123' (Fig. 3D-3E) that covers the dielectric films; and thinning a back surface of the semiconductor wafer 110 to make the trench sections penetrate to form through-vias. Brofman discloses that this process allows through-vias to be formed without breaking thin wafers and yet provides a process with highly competitive manufacturing cost (note paragraph 0010 and 0012). It would have been obvious to one of ordinary skill in the art to modify Poo-II by forming the through-holes/vias as taught by Brofman because such a modification would allow the "stacked structure" (in Poo-II) to be formed with relatively thin wafers, thereby reducing the overall height/dimensions of the device/module.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The references listed on the attached Form PTO-892 (not cited above) are cited to show semiconductor devices/modules having features similar to those in the current invention.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lex Malsawma whose telephone number is 571-272-1903. The examiner can normally be reached on Mon-Fri (8 hours between 5:30AM and 8:00 PM).

Art Unit: 2825

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lex Malsawma



August 30, 2004


CARIDAD EVERMOTT
PRIMARY EXAMINER